GaAs Monolithic MICs for Direct Broadcast Satellite Receivers

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ABSTRACT

A 12-GHz low-noise amplifier (LNA), a 1-GHz IF amplifier (IFA) and an 11-GHz dielectric resonator oscillator (DRO) have been developed for DBS home receiver applications by using GaAs MMIC (monolithic MIC) technology. Each MMIC chip contains FETs as active elements and self-biasing source resistors and bypass capacitors for single power supply operation. It also contains DC-block and RF-bypass capacitors.

The three-stage LNA exhibits 3.4-dB noise figure and 19.5-dB gain over 11.7 GHz-12.2 GHz. The negative-feedback type three-stage IFA shows 3.9-dB noise figure and 23-dB gain over 0.5 GHz-1.5 GHz. The DRO gives 10-mW output power at 10.67 GHz with a frequency stability of 1.5 MHz over a temperature range from -40 to 80 °C. A DBS receiver incorporating these MMICs exhibits an overall noise figure of ≤ 4.0 dB for frequencies from 11.7 to 12.2 GHz.

Introduction

Television broadcast systems via 12-GHz direct broadcast satellites (DBS) are scheduled to enter into operation in various countries in mid 1980's. Success of such systems, however, heavily depends on the availavility of low-noise 12-GHz receivers in large quantities at an acceptable price. In view of the potential of large-scale production and low cost, the GaAs monolithic microwave integrated circuit (MMIC) seems to be the most viable candidate for the receiver application.

Extensive efforts are being directed in various laboratories towards the development of GaAs MMICs for application to outdoor units of DBS receivers [1],[2],[3]. As shown in Fig. 1, a typical outdoor unit is composed of a GaAs FET low-noise amplifier (LNA), a band-pass filter, a mixer, an IF amplifier (IFA), and a dielectric resonator oscillator (DRO). This paper describes three kinds of FET-based GaAs MMICs (LNA, IFA and DRO) that have been developed for actual operation in an experimental outdoor unit. Each MMIC chip has been designed to operate under a single power supply by incorporating self-biasing resistors and capacitors and to have DC-block and RF-bypass capacitors. The LNA and IFA chips are mounted in ceramic package for easy handling, and the DRO chip is mounted in a hermetically sealed housing together with a dielectric resonator to avoid a moisture effect. The FETs and resistors in the IFA and DRO chips are fabricated by selective direct ion implantation into semi-insulating GaAs substrate. These MMICs have been successfully employed in an outdoor unit of a DBS home receiver. The following sections describe circuit design, fabrication, packaging and RF performance of the MMICs.

Circuit Design

(1) Low-Noise Amplifier (LNA)

The design goal was to build a low-noise amplifier with a noise figure of ≤ 3.5 dB and a gain of ≥ 20 dB at 12 GHz. In order to fulfil this goal, a three-stage FET amplifier was finally chosen. Prior to the three-stage design, however, a single-stage amplifier was built and thoroughly investigated for parameter study.

Figure 2 and Fig. 3 show the circuit diagram and the top view of the single-stage LNA chip, respectively. The chip measures 1.5 x 1.5 mm. A noise figure of an FET usually improves with shortening gate length as previously demonstrated by some of the present authors with a quarter-micron gate GaAs FET fabricated using electron beam lithography [4]. In the present work, however, the FET gate length is chosen to be 0.4 μm by making trade-offs between noise figure and device yield in the future production phase. The gate is also designed to have a width of 200 μm and a single pad to minimize the gate-source overlay parasitic capacitance. The source electrodes outside the FET are tapered to reduce the source inductance.

The optimum source and load impedances for gain and noise figure of the FET were determined by measuring S-parameters and noise parameters of a discrete FET equivalent to the FET to be employed in the MMIC. The discrete FET showed a minimum noise figure of 1.9 dB with an associated gain of 8.5 dB at 12 GHz. The input and output matching circuits of the single-stage LNA are designed to optimize a noise figure using the measured source and load impedances and realized by shunt- and series- connected microstrip lines with a characteristic impedance of 70 Ω. The shunt microstrip lines are terminated by RF bypass capacitors. Each length of the microstrip lines is compensated for by taking into account the effective line length reduction due to the coupling between lines. The thickness of the GaAs substrate has been chosen to be 300 μm by considering less matching circuit loss, easier chip handling and less performance changes

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due to thickness variation.

The source resistor Rs and RF bypass capacitor Cs are incorporated for single power supply operation. Rs is chosen to be 100 Ω to make drain current 7 mA at which the noise figure of FET reaches a minimum. An external gate bias terminal is also included in order to evaluate RF performance as a function of drain current. The capacitances of RF bypass capacitors, C_G and C_D, source capacitor C_S and DC block capacitor C_c are 8 pF, 15 pF and 4 pF, respectively.

After evaluation of the single-stage LNA, the three-stage LNA has been designed. The circuit diagram and the top view of the three-stage chip with a size of 1.5 x 3.0 mm are shown in Fig. 4 and Fig. 5, respectively. The input and output matching networks of each stage have been optimized for a source and load impedance of 50 Ω. The input matching circuits have been designed to optimize noise figure in the first and second stages and to optimize gain in the third stage. The source capacitor C_S and the resistor Rs are employed in every stage so that LNA can be operated under a single power supply. The capacitors, Cs, C_D and Cc and the resistors Rs have the same values as the corresponding ones in the single-stage LNA.

(2) IF Amplifier (IFA)

The IFA has been designed to give a noise figure of ≤ 3.5 dB, a gain of ≥ 20 dB and an input and output VSWR of ≤ 2.0 for frequencies from 0.5 to 1.5 GHz. Several approaches to the amplifier designs in this frequency range have been proposed to date [5],[6]. However, most of them are the ones that utilize a gate-drain resistive feedback at an individual FET with a relatively wide gate width. We have newly designed a three-stage monolithic IF amplifier, in which the feedback resistor is connected between the input and output ports of the amplifier. The circuit diagram and the top view of the IFA chip with a size of 1.5 x 1.5 mm are shown in Fig. 6 and Fig. 7, respectively.

In the amplifier design, considerations are also given to have easier assembly and operation in DBS receivers. The source resistors Rs and bypass capacitors Cs are incorporated as in the LNA for single power supply operation. Futhermore, the drain resistors R_D and bypass capacitor C_D are connected to each drain and at the bias feed terminal, respectively. The drain resistors R_D, together with the bypass capacitor C_D, make it possible to eliminate the RF choke otherwise necessary outside the chip, and improve the gain flatness and stability of the amplifier at a sacrifice of gain. The gate of each FET has a length of 1 μm. By using a computer simulation, its width is optimized to be 600 μm as well as the gate resistors R_{G1}, R_{G2} and R_{G3}, the drain resistors R_D and the feedback resistor R_F in terms of noise figure, gain flatness and input and output VSWRs. The capacitor values are determined such that the performance does not degrade at lowest frequencies of interest.

(3) Dielectric Resonator Oscillator (DRO)

The local oscillator for DBS receiver applications is required to have a superior frequency stability such as ± 1 MHz for a center frequency of 10.7 GHz over a wide temperature range from -40 to 80 °C. Among several types of MMIC oscillators proposed to date [7],[8], the dielectric resonator oscillator configuration is the most promising candidate for the local oscillator application in view of size and cost. We have designed a dielectric resonator oscillator which consists of an MMIC oscillator chip and a dielectric resonator circuit. The oscillator circuit diagram and the top view of the oscillator chip with a size of 1.5 x 1.5 mm are shown in Fig. 8 and Fig. 9, respectively.

The hybrid MIC technology is used to form the resonant circuit for frequency stabilization. The dielectric resonator is mounted on an alumina substrate and coupled to a microstrip line terminated by a 50-Ω load. The dielectric resonator used has an unloaded Q of 7,400, a relative dielectric constant of 36.3 and a resonant-frequency temperature coefficient of +6 ppm/°C.

The MMIC oscillator chip has a common-source configuration with a feedback capacitor Cs. The FET with a gate length of 1 μm and a width of 300 μm is used in order to obtain an oscillator output power of 10 dBm. The circuit parameter design has been performed by using the measured S-parameters of the equivalent discrete FET. The feedback capacitor Cs of 0.3 pF is determined by a computer simulation so as to make the output reflection coefficient at the drain terminal maximum under a given reflection coefficient of the resonant circuit with a loaded Q of 1,000. The output matching circuit is optimized by a nonlinear analysis based upon the measured large signal impedance of the discrete FET. It is composed of a series microstrip line and a shunt microstrip line terminated by the RF bypass capacitor C_D.

The resistor Rs with a quarter-wavelength shunt stub is used for single power supply operation. Rs of 50 Ω is chosen to make drain current 20 mA. The drain bias circuit is included in the output matching circuit. The bypass capacitor C_D and DC-block capacitor Cc have the capacitance of 12 pF and 8 pF, respectively.

Device Fabrication

The LNA chip is fabricated, using an epitaxial wafer with active and buffer layers successively grown on Cr-doped semi-insulating substrate by a metal-organic chemical vapor deposition method. The carrier concentration and thickness of the active layer are 2.0×10^{17} cm^{-3} and 0.5 μm, respectively. Mesas are formed to define the FET active areas and resistors.

On the other hand, the IFA and the DRO MMICs are fabricated by selective Si ion implantation into undoped semi-insulating GaAs substrate. A resist / SiO_2 film is used as a mask for the ion implantation. The accelaration energy and dose were 70 keV and 3.5×10^{12} cm^{-2} for FET active layers. For FET contact layers and resistor layers, Si ions are dually implanted at a dose of 2×10^{13} cm^{-2} and energies of 250 keV and 120 keV. After ion implantation and removal of the resist / SiO_2 film, the wafers were annealed at 850 °C for 15 minutes in AsH_3 / Ar atmosphere without encapsulants.

The gate of the FETs in the LNA is defined to a length of 0.4 μm and a width 200 μm by using an

electron beam lithography. The gate is recessed in order to attain a low noise figure. The gate length of FETs in the IFA and DRO MMICs is 1 μm, and the widths are 600 μm and 300 μm, respectively. They were delineated by a conventional photolithography.

The Schottky barrier gate electrodes are formed by Al with a thickness of 6000 Å. The ohmic electrodes are formed by alloying Pt / AuGe at 450 °C. The first level metallization of the MIM capacitor is 0.8-μm thick Al. CVD SiO_2 film with a thickness of 3,500 Å is used as the capacitor dielectric. The Au / Pt / Ti metal systems are used for the top plates of the capacitors, the bonding pad and the interconnection metals. All of the metal patterns are formed by a lift-off process.

The MMIC chips are all glassivated with a CVD SiO_2 film, except for the bonding area. After lapping the substrate to a thickness of 300 μm, the backside of the wafer is metallized.

Device Packaging

For evaluation of the LNA and IFA MMICs in a DBS receiver, a specially designed universal hermetic package has been provided. It is a rectangular stripline package with a copper flange. The packaged LNA and IFA are shown in Fig. 10 (a) and (b), respectively, with top covers removed. The LNA contains a three-stage LNA chip. The IFA contains two cascaded three-stage IFA chips. The two center leads are for RF input and output. While other leads can be used for DC biasing, only one of them is employed in the present application since the MMIC chips are designed for single power supply operation. The DC bias connection to the chips is done via a dielectric standoff. The DRO chip has been mounted together with a dielectric resonator in a hermetically sealed MIC housing with outer dimensions of 25 x 25 x 12 mm.

RF Performance

(1) Low-Noise Amplifier (LNA)

Figure 11 shows the measured frequency response of noise figure and gain of the single-stage LNA at a drain voltage V_{DD} = 4 V and a drain current I_D = 8 mA. The MMIC chip is mounted on a coplanar test fixture. A minimum noise figure of 2.8 dB and a gain of 6.5 dB are obtained at 12 GHz.

The three-stage LNA chip was evaluated after mounting it into the hermetic ceramic package as shown in Fig. 10 (a). Figure 12 shows the measured frequency response of noise figure and gain of the LNA operated at V_{DD} = 4 V and a total current I_D = 25 mA. A minimum noise figure of 3.4 dB and a gain of 20 dB are obtained at 12 GHz, and a noise figure ≤ 3.4 dB and a gain ≥ 19.5 dB are obtained at frequencies from 11.7 to 12.2 GHz. The minimum noise figure and the gain are in good agreement with the values predicted from the single-stage LNA performance. The frequency of maximum gain, however, is shifted towards lower frequency. This might be caused by an insufficient interstage matching.

Figure 13 shows the measured frequency response of input and output return losses of the three-stage LNA. An input return loss ≥ 6 dB (VSWR ≤ 3.0) and an output return loss ≥ 12 dB (VSWR ≤ 1.7) are obtained at frequencies from 11.7 to 12.2 GHz. The input VSWR characteristic is found similar to that of the single-stage LNA measured using the coplanar test fixture. However, the output VSWR is found worse than that of the single-stage LNA. The disagreement is due to the dimensional limitation of the ceramic package. The inner dimension of the package is around one and a half times longer than the MMIC chip length. Since the MMIC chip has been mounted at the input terminal side of the package, long bonding wires are used to connect the output pad of the chip and the output terminal of the package. The bonding wire has an inductance of ~1.0 nH, causing the output VSWR discrepancy between the measurement and design.

(2) IF Amplifier (IFA)

The three-stage IFA chip was also evaluated after mounting it into the hermetic ceramic package. Figure 14 shows the measured frequency response of noise figure and gain of the IFA operated at a drain voltage V_{DD} = 7 V and a total current I_D = 39 mA. A noise figure ≤ 3.9 dB and a gain 23.5 ± 0.1 dB are obtained at frequencies from 0.5 to 1.5 GHz. The measured performance shows a good agreement with the simulation result.

Figure 15 shows the measured frequency response of input and output return loss. An input return loss ≥ 7 dB (VSWR ≤ 2.6) and an output return loss ≥ 11 dB (VSWR ≤ 1.8) are attained in the same frequency band. Although the IFA has been designed to minimize the input and output VSWRs at a center frequency of 1 GHz, the measured minimum input and output VSWRs are shifted towards lower frequencies. A computer simulation can explain this discrepancy if we assume that gate-source capacitance of actual FET is larger by a factor of 1.3 than the one used in the design.

The output power at 1-dB gain compression point and the third-order intercept point of the IFA are measured to be 8 dBm and 18 dBm, respectively, at 1 GHz.

Since an IF amplifier gain of ≥ 40 dB was required to operate the outdoor unit to be tested, two IFA chips have been cascade-mounted in the package as shown in Fig. 10 (b). The measured gain of the cascaded IF amplifier is 45 ± 0.3 dB over 0.5 - 1.5 GHz, and the input and output VSWRs are found similar to those of the single chip IFA.

(3) Dielectric Resonator Oscillator (DRO)

Figure 16 shows the measured drain voltage (V_{DD}) dependence of output power (Pout), oscillation frequency deviation (Δf) and efficiency (η) of the DRO with a center oscillation frequency of 10.67 GHz. An output power of 10.5 dBm with 10 % efficiency is obtained at a drain voltage V_{DD} = 5 V. The frequency pushing is ~0.2 MHz / V. Since the measured frequency pulling for VSWR = 1.5 is ~400 kHz, the external Q of the DRO is calculated to be ~10,000.

Figure 17 shows the temperature dependence of frequency deviation (Δf) and the output power (Pout). It is found that the frequency variation is 1.5 MHz (1.2 ppm / °C) and the output power variation is 4 dB over a temperature range from -40 to 80 °C.

DBS Receiver Application

An outdoor unit of DBS receiver has been modified to accommodate the developed LNA, IFA and DRO MMICs. The packaged LNA containing a three-stage chip and the packaged IFA containing two cascaded three-stage chips have been employed. The outdoor unit has exhibited an overall noise figure of $\leq$ 4 dB for frequencies from 11.7 to 12.2 GHz.

Conclusion

Three kinds of GaAs MMICs have been developed for a DBS receiver application. Bearing this application in mind, efforts have been made in designing MMICs to operate under single power supply without any special RF choking, and in packaging, as well as in other design considerations. An MMIC mixer is now under development.

Although the 4-dB noise figure of the tested DBS receiver is a very encouraging result, much has yet to be done before GaAs MMICs are used in quantities in an actual production line of DBS receivers. The key to meet such a large-scale production phase lies in good-quality large-diameter semi-insulating GaAs substrates, high-yield wafer processing, high-speed automated testing and low-cost packaging, as well as in good performance MMIC design.

Acknowledgement

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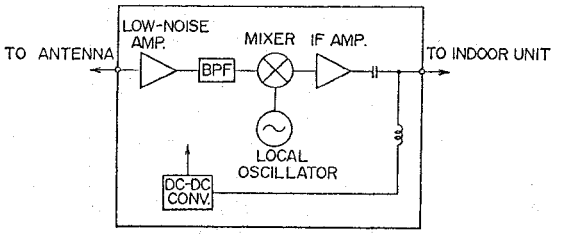
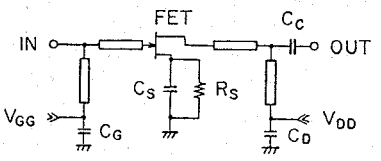


Fig. 1. Typical block diagram of outdoor unit of DBS receiver.



R_S = 100 Ω
C_S = 15 pF
C_G = C_D = 8 pF
C_C = 4 pF

Fig. 2. Circuit diagram of single-stage low-noise amplifier.

References

[1] C. Kermarrec, P. Harrop, C. Tsironis and J. Faguet, " Monolithic Circuits for 12 GHz Direct Broadcasting Satellite Reception, " in 1982 IEEE MTT Monolithic Circuit Symp. Dig., pp. 5 - 10.

[2] R.A. Pucel, " Design Considerations for Monolithic Microwave Circuits, " IEEE Trans. MTT , vol. MTT-29, No.6, pp. 513 - 534, June 1981.

[3] L.C. Liu, D.W. Maki, M. Feng and M. Siracusa, " Single and Dual Stage Monolithic Low Noise Amplifiers, " in 1982 GaAs IC Symp. Dig., pp. 94 - 97.

[4] K. Kamei, S. Hori, H. Kawasaki and T. Chigira, " Quarter Micron Gate Low Noise GaAs FETs Operable up to 30 GHz, " in 1980 IEDM Dig., pp. 102 - 105.

[5] K. Honjo, T. Sugiura, T. Tsuji and T. Ozawa, " Low-Noise, Low-Power-Dissipation GaAs Monolithic Broadband Amplifiers, " in 1982 GaAs IC Symp. Dig., pp. 87 - 90.

[6] S. Hori, K. Kamei, M. Tatematsu, T. Chigira, H. Ishimura and S. Okano, " Direct-Coupled GaAs Monolithic IC Amplifiers, " in 1982 IEEE MTT Monolithic Circuit Symp. Dig., pp. 16 - 19.

[7] J.S. Joshi, J.R. Cockrill and J.A. Turner, " Monolithic Microwave Gallium Arsenide FET Oscillators, " IEEE Electron Device, vol, ED-28, No.2, pp. 158 - 165, February 1981.

[8] B.N. Scott, G.E. Brehm, " Monolithic Voltage Controlled Oscillator for X and Ku-Band, " in 1982 IEEE MTTs Int. Microwave Symp. Dig., pp. 482 - 485.

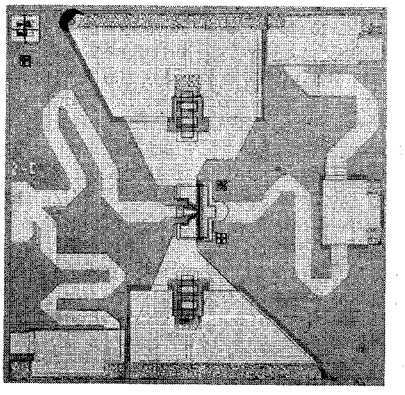


Fig.3. Single-stage low-noise amplifier chip (1.5 x 1.5 mm)

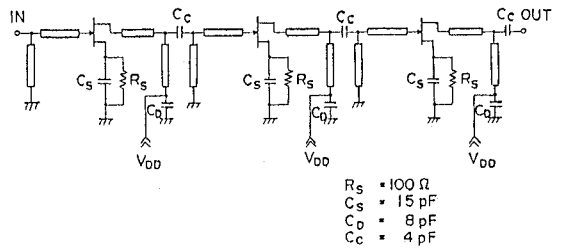


Fig. 4. Circuit diagram of three-stage low-noise amplifier.

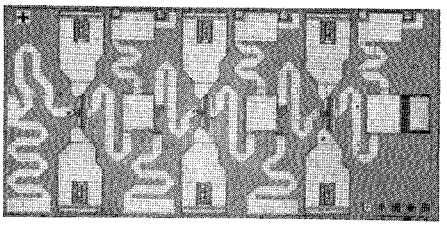


Fig. 5. Three-stage low-noise amplifier chip (1.5 x 3.0 mm).

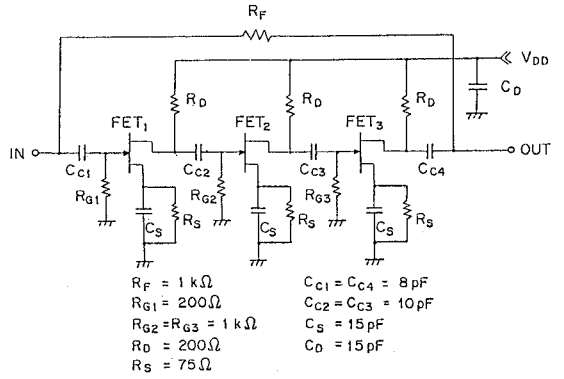


Fig. 6. Circuit diagram of 1 GHz IF amplifier.

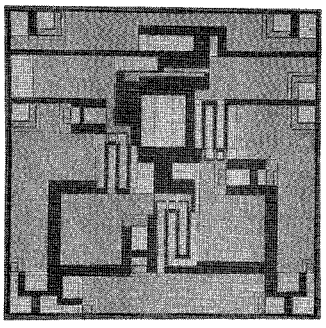


Fig. 7. IF amplifier chip (1.5 x 1.5 mm).

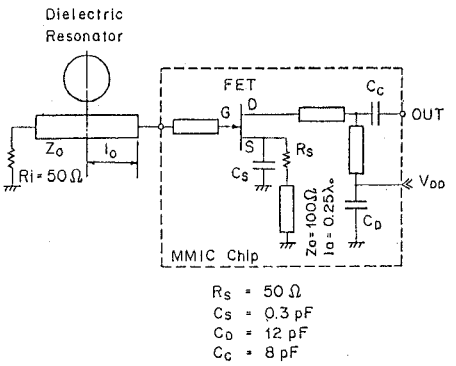


Fig. 8. Circuit diagram of dielectric resonator oscillator.

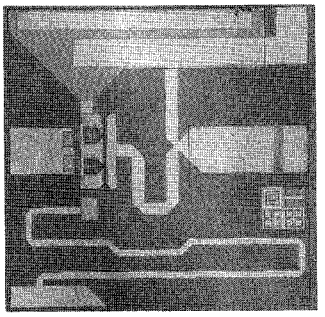


Fig. 9. Dielectric resonator oscillator chip (1.5 x 1.5 mm).

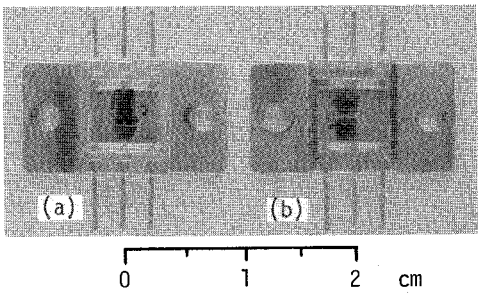


Fig. 10. Inside view of packaged (a) LNA and (b) IFA.

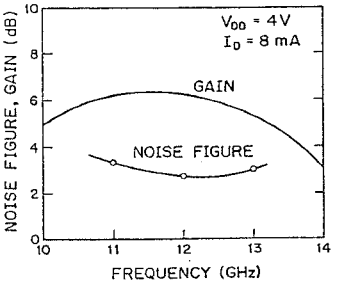


Fig. 11. Measured noise figure and gain of single-stage low-noise amplifier as a function of frequency.

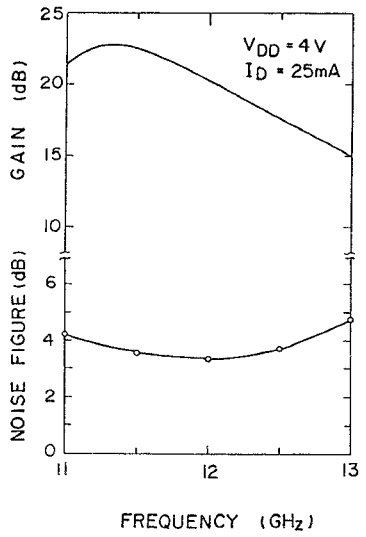


Fig. 12. Measured noise figure and gain of three-stage low-noise amplifier as a function of frequency.

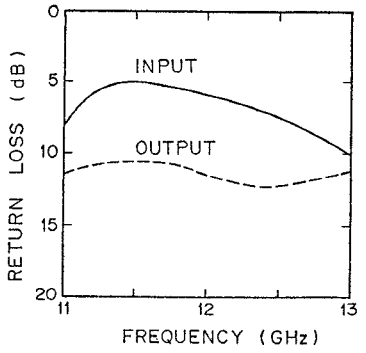


Fig. 13. Measured input and output return loss of three-stage low-noise amplifier as a function of frequency.

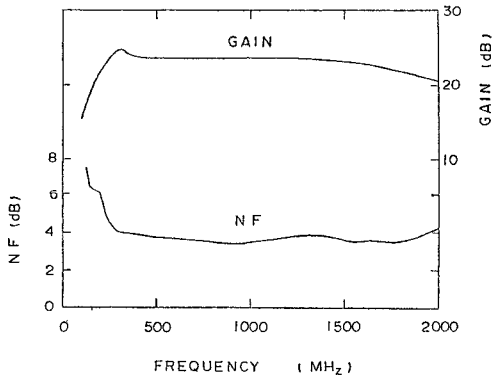


Fig. 14. Measured noise figure and gain of 1 GHz IF amplifier as a function of frequency.

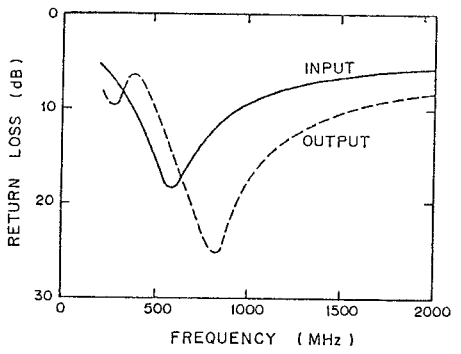


Fig. 15. Measured input and output return loss of 1 GHz IF amplifier as a function of frequency.

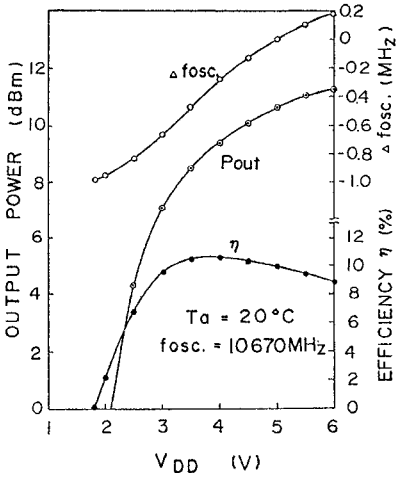


Fig. 16. Measured output power (Pout), oscillation frequency (Δfosc) and efficiency (η) of dielectric resonator oscillator as a function of drain voltage (V_{DD}).

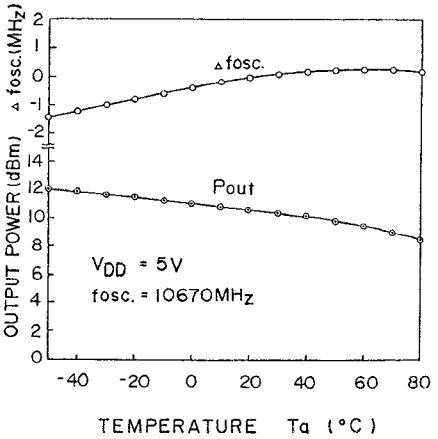


Fig. 17. Measured temperature dependence of oscillation frequency deviation (Δfosc) and output power (Pout) of dielectric resonator oscillator .